
DEPARTMENT OF
ELECTRONICS AND COMMUNICATION ENGINEERING

A Report

One week SDP on

"VLSI PHYSICAL DESIGN FLOW: RTL to GDSII"

From 18/06/2024 to 22/06/2024

The Research Group NIVAG-Department of ECE successfully conducted a week workshop on " **VLSI PHYSICAL DESIGN FLOW: RTL to GDSII**" for III B.Tech. Students from 18th June 2024 to 22nd June 2024. This workshop aims to provide insight into the importance of Xilix-Vivado and Cadence Software and its related tools for student development in the field of VLSI Design. The workshop comprises of theoretical lectures and demonstrations of the software and Design Implementations by department faculties.

The students got exposure to Verilog coding and design Implementation on FPGA boards. As an outcome of the workshop, the students can develop programming code, can implement them on FPGA Boards. They can able to simulate and synthesis.

Totally 43 students participated in the workshop and it was organized in association with **the IETE Student Forum (ISF).**

Mrs V.V.Nandini & Mr.K.Ramesh, worked as Faculty Coordinators for this workshop.

NIVAG Research group with Dean, and HoD

On 18th June 2024:

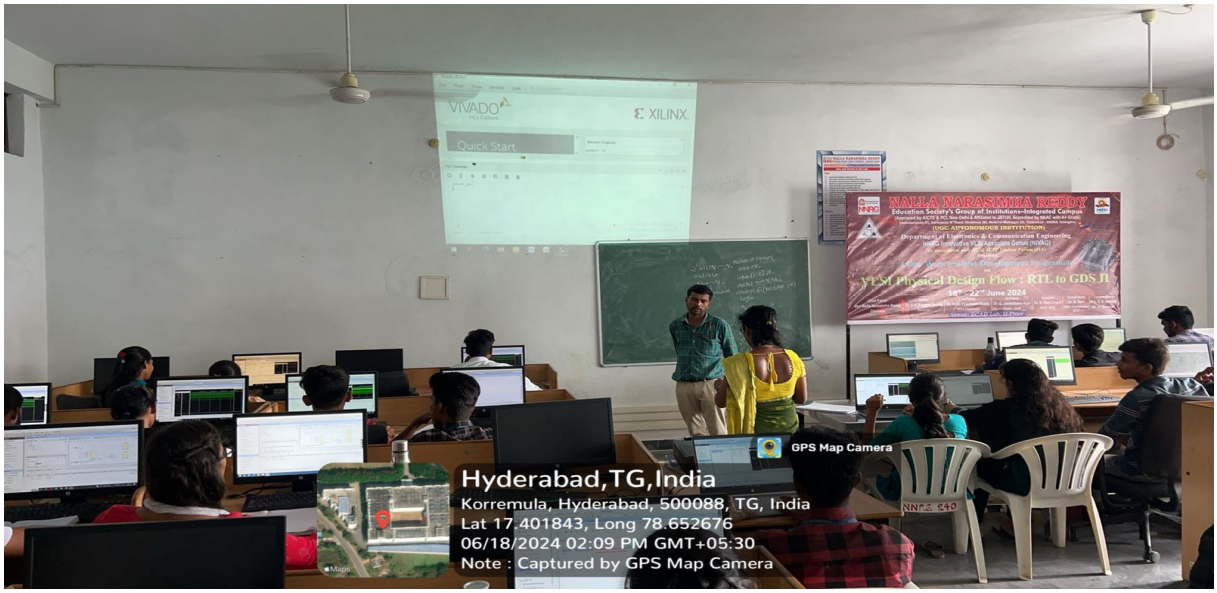
Day-1 INAUGURATION (10:00 am to 11 am):

The workshop was inaugurated by Director, Dean-School of Engineering, and ECE-Head at the ECE seminar hall from 10:00 am to 11 am.

NIVAG Research group with Dean, and HoD

Day-1 Forenoon (11:15 am to 12:50 pm) ;

The workshop started from forenoon session 2 in which **Mr.K.Srinivas** delivered the lecture on **"Design of Sequential Circuits"** and related concepts. The afternoon session is followed by hands-on training using Xilinix-Vivado.



Mr.K.Srinivas, Assistant Professor as resource person delivered the concepts of

"Design of Sequential Circuits"

Day 1 Afternoon (1:30 pm to 4:00 pm)::

In the morning session, **Mr.K.Ramesh** handled the practical session on **"FPGA implementation of Sequential Circuits"** followed by practical sessions in the afternoon.

Mr.K.Ramesh, Assistant Professor of ECE, as a resource person delivered the concept of "**FPGA implementation of Sequential Circuits**".

Day 2 Forenoon and Afternoon Session:

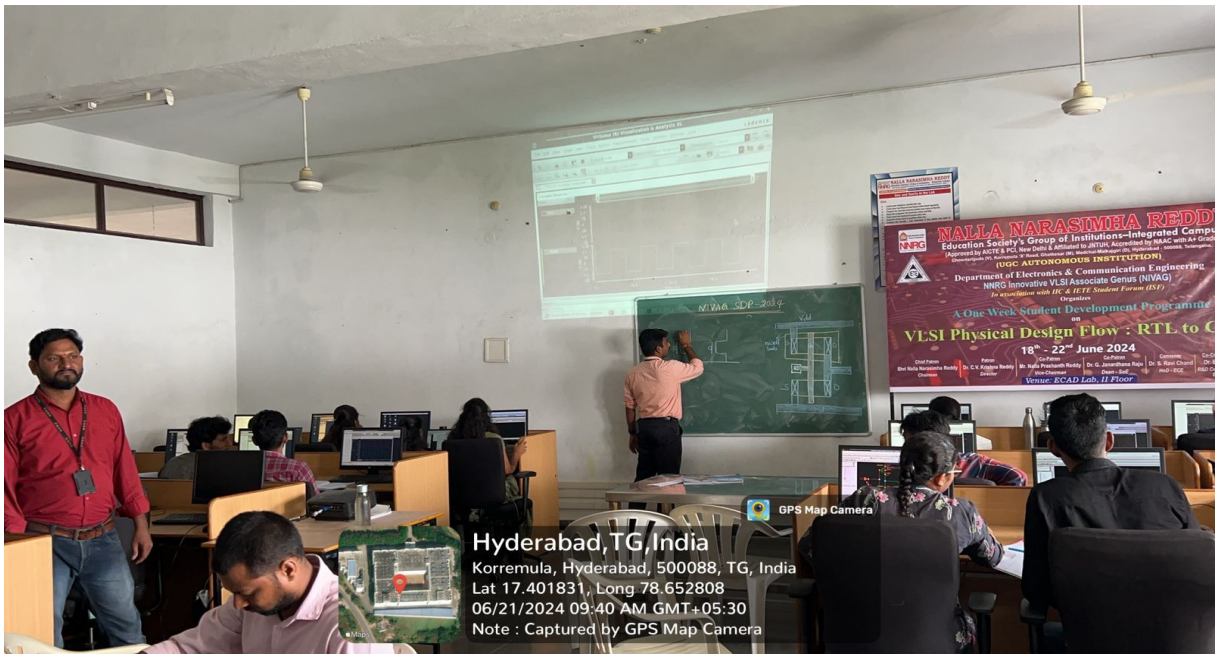
In the morning session and Afternoon session, Mrs V.V.Nandini and Mrs N.Lavanya handled the theoretical session on "**Design Of FSM**"followed by practical sessions in the afternoon.

Mrs N.Lavanya, Assistant Professor of ECE, as a resource person delivered the concept of

"**Design Of FSM**".

Day-3 Forenoon and Afternoon Session:

In morning session, resource person **"Dr.B.Hariprasad Naik"** delivered practical session on **"Basic IP Core& Implementation On FPGA".**



Dr.B.Hariprasad Naik, Associate Professor of ECE, delivered the concept of

"**Basic IP Core& Implementation On FPGA".**

Day-4 Forenoon and Afternoon Session

In afternoon session, resource person **"Dr.B.Hariprasad Naik"** delivered practical session on **"Introduction to Cadence Virtuoso Design Flow".**

Dr.B.Hariprasad Naik, Associate Professor of ECE, delivered the concept of "**Introduction to Cadence Virtuoso Design Flow**".

Day-5 Forenoon Session:

In the morning session, resource person Mrs.**V.V.Nandini** delivered a lecture on **" IC Design Using Cadence Virtuoso".** The afternoon session is followed by hands-on implementation.

Ms.V.V.Nandini, Assistant Professor of ECE delivered lecture on **IC Design Using Cadence Virtuoso**

Day-5 Afternoon session (Valedictory):

The valedictory program is organized during the afternoon session. The program is felicitated by Dean and Hod-ECE.

Director Sir, NNRG addressing the students and the faculties

I/C HOD - ECE, NNRG addressing the students and the faculties

Student participants receiving merit certificates from Director Sir – A Glimpse

Outcomes of the Workshop:

After the completion of workshop, the students are able to Code a program in the Xilinx-Vivado, and Cadence Can design, Simulate & Synthesis on FPGA implementation.

1) FPGA implementation of Sequential Circuits
2) FPGA implementation of FSM
3) IC Design Using Cadence Virtuoso
4) Basic IP Core& Implementation on FPGA
5) Advance IP Core& Implementation on FPGA

Place: Hyderabad
Date: 22/06/2024

NIVAG - SPoC **R&D COORDINATOR** **HOD-ECE**